

Date **Rev** **By** **History**

V0.26 8/28/2024 BMc **PDN-3A Diag only**

- 1. Created new J742S2 EVM PDN-3A detailed block diagram from primary universal PDN-3x reference file “J784S3 EVM ...PDN-3A” v0.26.
- 2. Differences vs J784S4 listed:
 - a. Replace SoC with J742S2 block with Pkg code & ball count updated for 27x27mm
 - b. Remove “SERDES 2” from combined input supply.



Legend:

Power Rails	Control Signals:	
<p>PDN base</p> <p>MCU Only/Safety Island</p> <p>GPIO Retention</p> <p>DDR_Retention (aka S2R)</p> <p>End Product option</p> <p>Peripheral loads (SW config'd after boot)</p>	<p>General ctrlr & logic (Italic = SW config'd after boot)</p> <p>PDN base ctrlr</p> <p>Func Safety</p> <p>MCU Only/Island</p> <p>GPIO Retention</p> <p>DDR_Retention (aka S2R)</p> <p>End Product option</p> <p>Peripheral comps</p> <p>Debug/Development option</p>	<p>Note items</p> <p>On-Chip "Pwr OK" Monitors (OV & UV)</p> <p>On-Chip "Pwr OK" Monitors (UV only)</p> <p>Provisioned In-Line Supply Filter</p> <p>High-lighted diagram changes</p>

Leo PMIC-A, PN TPS6594**133A**RWERQ1 (Ti PN ID = **1**, MP Buck Rails = **3**, PG2.0 NVM ID = **3A Rev 5**)
 HCPS-A & B, Tulip PN TPS6287**3Y1Q**WRXSQR1 (15A PN ID = **3**, Jacinto7 Family ID = **Y1**)
 Safety Voltage Supervisor, PN TPS38900**6004R**TERQ1 (OTP ID = **004** = new common PN for use with Jacinto7 178454 PDN-3A scheme)

J784S4 EVM Leo + 2x High-Current Pwr Stages(HCPS) PDN-3A

(All SoC PN variants: TDA4AP/VP/AH/VH)

(Power Rail & GPIO Mapping Overview)

V0.26 5/21/2024

1. Created J742S2 EVM PDN-3A detailed PDN diagram from J784S4 EVM PDN-3A v0.26 diagram.
2. Modified SoC block to show J742S2 package differences and removal of SERDES2 analog supply inputs.

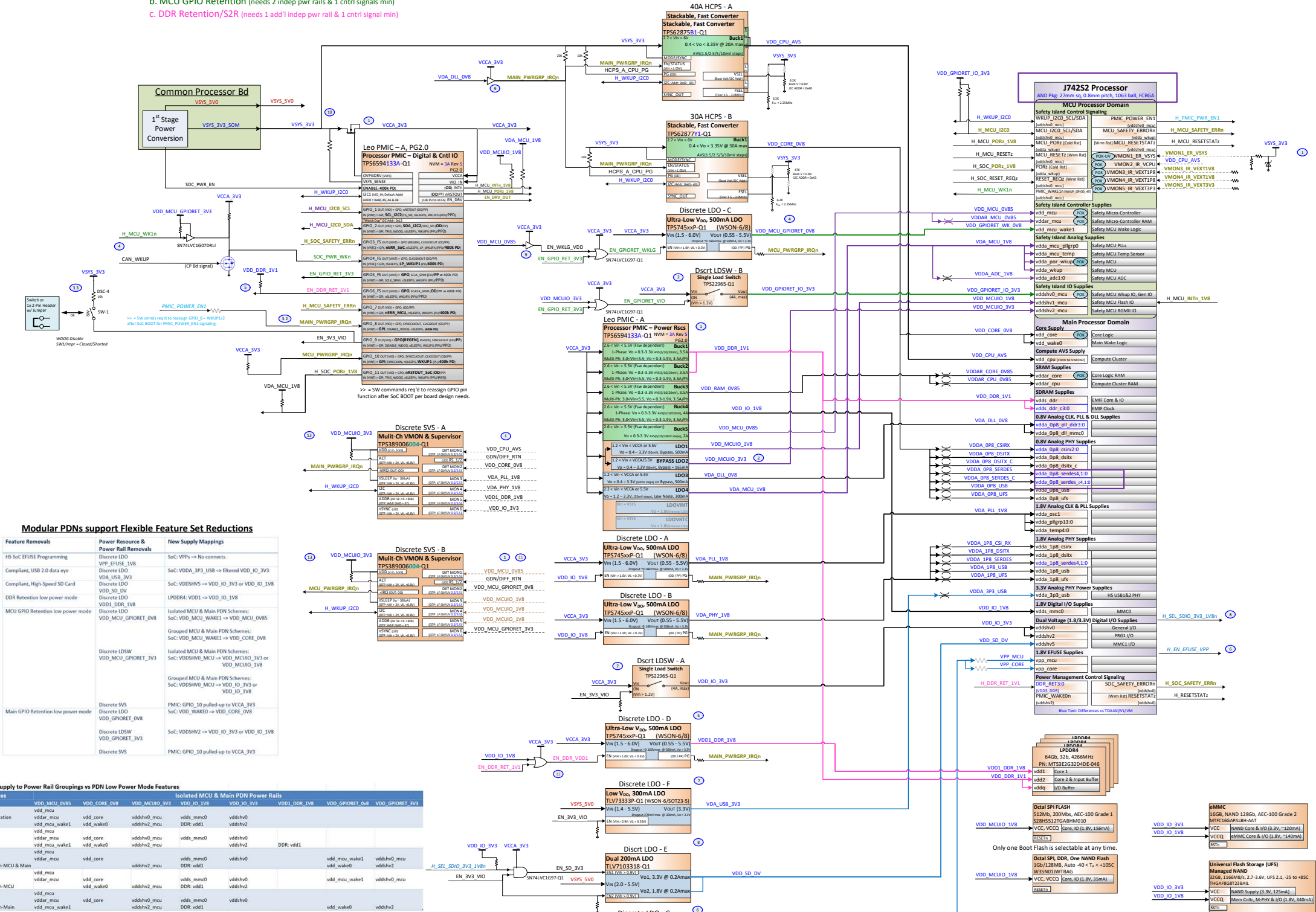
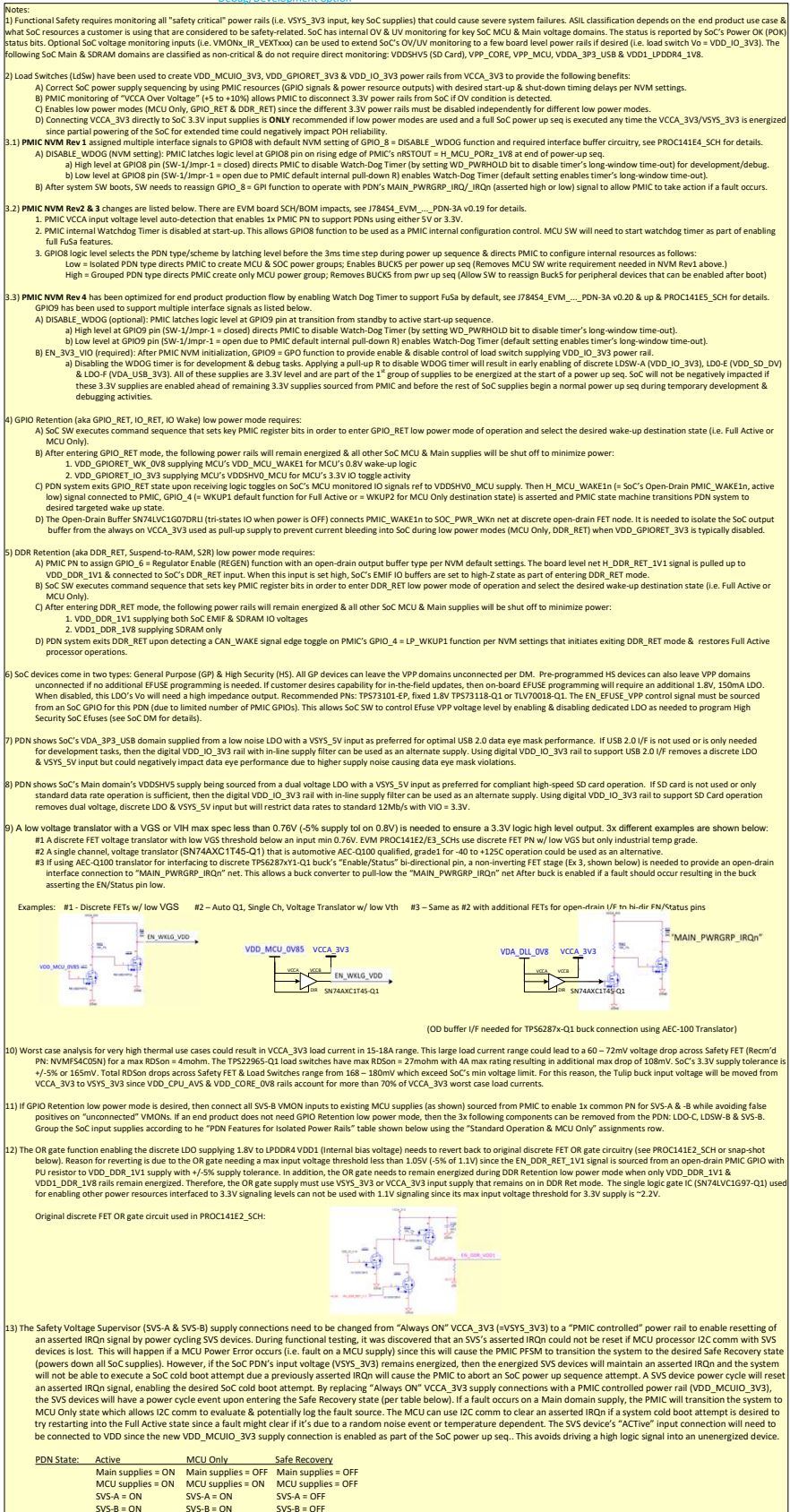
Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable sys w/ isolated Main & MCU power rails (supply FFI)
3. 4x SDRAMs: 32Gb, 4-Die, 32b, 426mMTs, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash & eMMC, UFS
5. Signaling Levels: MCU & Main Dual VIO
6. Low power modes:

- a. MCU Island/Only with Dual VIO (needs 4 indep pwr rails & 1 cntrl signal min)
- b. MCU GPIO Retention (needs 2 indep pwr rails & 1 cntrl signals min)
- c. DDR Retention/S2R (needs 1 add'l indep pwr rail & 1 cntrl signal min)

- ## 7. End Product Options:

- a. Compliant high-speed SD Card (needs 1 indep pwr rail & 1 VIO cntrl signal & discrete LDO needs Vin = 5V)
- b. Compliant USB 2.0 data eye (needs 5V, 1 indep pwr rail & discrete LDO needs Vin = 5V)
- c. HS SoC Efuse programming on-board (needs 1 indep pwr rail & 1 cntrl signal)



Modular PDNs support Flexible Feature Set Reductions

Feature Removals	Power Resource & Power Rail Removals	New Supply Mappings
HS SoC FUSE Programming	Discrete DDO VPP, F10SE_1V8	SoC: VPPs → No connects
Compliant, USB 2.0 data eye	Discrete DDO VDDA_1V8, V3V3	SoC: VDDA_3V3_1V8 → filtered VDD_IO_3V3
Compliant, High-Speed SD Card	Discrete DDO VDDA_1V8, V3V3	SoC: VDD0V5H5 → VDD_IO_3V3 or VDD_IO_1V8
DDR Retention low power mode	Discrete DDO VDD1_0D8_1V8	LPDDR4: VDD1 → VDD_IO_1V8
MCU GPIO Retention low power mode	Discrete DDO VDD1_MCU_GPIORET_0V8	Isolated MCU & Main PDM Schemes: SoC: VDD1_MCU_WAKE1 → VDD1_MCU_0V85
		Grouped MCU & Main PDM Schemes: SoC: VDD1_MCU_WAKE1 → VDD_CORE_0V8
	Discrete LDDW VDD1_MCU_GPIORET_3V3	Isolated MCU & Main PDM Schemes: SoC: VDD0V5H5_MCU → VDD1_MCU0V3V3 or VDD1_MCU0V1V8
		Grouped MCU & Main PDM Schemes: SoC: VDD0V5H5_MCU → VDD1_IO_3V3 or VDD1_IO_1V8
Main GPIO Retention low power mode	Discrete SVS Discrete DDO VDD1_GPIORET_0V8	PMIC: GPIO_10 pulled-up to VCCA_3V3 SoC: VDD1_WAKE0 → VDD1_CORE_0V8
	Discrete LDDW VDD1_GPIORET_3V3	SoC: VDD0H22 → VDD1_IO_3V3 or VDD1_IO_1V8
	Discrete SVS	PMIC: GPIO_10 pulled-up to VCCA_3V3

Supply to Power Rail Groupings vs PDN Low Power Mode Features

		Isolated MCU & Main PDI Power			
		VDD_MCU_0V18	VDD_CORE_0V18	VDD_MCU0V_3V3	VDD_I/O_1V8
Operation	VDD_MCU_0V18	vddr_core	vddshv2_mcu	vddr_vddm0	vddshv0
	vddr_mcu_wake1	vddr_wake0	vddshv2_mcu	DDR_vdd1	vddshv2
	VDD_MCU_0V18	vddr_core	vddshv2_mcu	vddr_vddm0	vddshv0
	vddr_mcu_wake1	vddr_wake0	vddshv2_mcu		vddshv2
MCU & Main	VDD_MCU_0V18	vddr_core		vddr_vddm0	vddshv0
	vddr_mcu		vddshv2_mcu	DDR_vdd1	
	VDD_MCU_0V18	vddr_core		vddr_vddm0	vddshv0
	vddr_mcu	vddr_wake0	vddshv2_mcu	DDR_vdd1	vddshv2
MCU	VDD_MCU_0V18	vddr_core		vddr_vddm0	vddshv0
	vddr_mcu_wake1				
	VDD_MCU_0V18	vddr_core		vddr_vddm0	vddshv0
	vddr_mcu_wake1				

Notes:

- 1) Power rail names shown in "ALL CAPITAL LETTERS"
- 2) SoC input supplies shown in "all lower case letters"

TPS6594133A NVM | Revision History

Revision	Release Date
0.0	April 25, 2022
1.0	August 8, 2022
2.0	October 10, 2022
3.0	December 15, 2022
4.0	Only released in sample units
5.0	March 1, 2024

TPS6594133A NVM | Revision Details

Rev	Change	Impact of Change
1.0	GPIO Retention Entry/Exit Handling – If Wake signal triggers while being armed, PMIC will enter Retention and then immediately ext.	Prevents PMIC from getting stuck in Retention
	Power Down Sequence Timing Changes -Updated power down seq of VDA_DLL_0V8 to shift disabling from 2.5ms to 1.0ms due to ~1ms delay in VDA_DLL_0V8 RC discharge before VDD_CPU_AV5 & VDD_CORE_0V8 are disabled by VDA_DLL_0V8 dropping below 0.6V FET Von threshold. -Updated power down seq of VDD_MCU_0V85 to shift disabling from 2.5ms to 2.0ms to ~align with disabling of VDD_CPU_AV5 & VDD_CORE_0V8.	Overall sequence time remains the same. Better power down seq when using discrete component rails to align with J7 SoC DM recommended seq.
	At startup, all PMIC power resources/rails mapped to a single MCU_PWR_ERR group	<ul style="list-style-type: none">Enables 1x PMIC PN to support both Grouped & Isolated PDN board designsGrouped MCU & Main PDNs (3G to 3M) need 1x PMIC power group to enable fault on any monitored rail to cause an orderly shutdown.Isolated MCU & Main PDNs (3A to 3F) will need MCU SW to create 2x power groups (MCU & Main) by writing 0x1E to PMIC register 0x44

TPS6594133A NVM | Revision Details

Rev	Change	Impact of Change
2.0	VCCA Input voltage level auto-detection	Enables 1x PMIC PN to support PDNs with VCCA voltage of 5V or 3.3V
	Watchdog Timer disabled	<ul style="list-style-type: none">GPIO8 used for PMIC config controlMCU SW will need to start watchdog timer as part of enabling full FuSa features
	GPIO8 logic level latched before 3ms time step of power up sequence & directs PMIC to configure internal resources: <ul style="list-style-type: none">Low = Creates 2x power groups; Enables BUCK5 per power up seqHigh = Creates 1x power group; Removes BUCK5 from power up seq	<ul style="list-style-type: none">Isolated MCU & Main PDNs (3A to 3F) need 2x power groups, use Buck5 for VDD_MCU_0V85 rail & connect MAIN_PWRGRP_IRQn to GPIO8 for discrete power resource monitoring.Grouped MCU & Main PDNs (3G to 3M) need 1x power group, removes Buck5 from pwr up seq (Buck5 can be reassigned by SW config to supply a peripheral rail after SoC & SW boot-up) & connects GPIO8 to pull-up resistor to set logic high.

TPS6594133A NVM | Revision Details

Rev	Change	Impact of Change
2.0	Removed any2ota sequence	PMIC OTA preparation sequence is no longer available. Unused during normal operation.
	Fixed GPIO10 response during normal operation	Prevents PMIC from getting stuck after MCU_PWRGRP_IRQn triggers a recovery attempt
3.0	Adjusted internal setting for improved BUCK reliability	No impact to function

TPS6594133A NVM | Revision Details

Rev	Change	Impact of Change
4.0	Watchdog enabled by default with 1 sec long window	MCU SW must boot and configure watchdog within 1 second of nRSTOUT going high
	Change default GPIO9 function from GPIO to WD_DISABLE	GPIO9 starts as an input to set WD_PWRHOLD bit, then changes to an output. In Development: Customer has <i>option</i> to use external PU resistor to set WD_PWRHOLD =1 In End Equipment: No impact to function
	TO_ACTIVE sequence has 500us delay between LDO3 and BUCK5	In systems with split power groups, PMIC BUCK5 powers up fully before PMIC LDO3. Overall sequence time remains the same.
	LDO2 OV/UV Threshold changed from 5% to 10%	When used as 3.3V load switch, PG Window will match that of VCCA. Customer can tighten after boot.

*Error found EN_I2C_CRC sequence, only on Rev4

TPS6594133A NVM | Revision Details

Rev	Change	Impact of Change
5.0	Watchdog Long Window set to 13 minutes.	MCU SW must boot and configure watchdog within 13 minutes of nRSTOUT going high
	Fixed EN_I2C_CRC sequence error	MCU can use I2C_2 FSM Trigger to enable I2C CRC

NVM Rev 4 Summary of Changes

Clarifications

Item	Change	Impact
1	Watchdog enabled by default with 1 sec long window	MCU SW must boot and configure watchdog within 1 sec of nRSTOUT (SoC's MCU_PORz) going high
2	Change GPIO9's default NVM function from GPI to WD_DISABLE	GPIO9 starts as an input to set WD_PWRHOLD bit, then changes to an output. In Development/Debug: Customer has option to use external PU resistor to disable WD Timer by setting WD_PWRHOLD =1 In End Equipment: WD Timer enabled by default
3	TO_ACTIVE sequence adds 500us delay to LDO3 enable	Adds timing margin to ensure BUCK5 (SoC's VDD_MCU_0V85) powers up fully before Tulip buck (SoC's VDD_CORE_0V8) that is enabled by LDO3
4	LDO2 output OV/UV Threshold changed from 5% to 10%	When used as 3.3V load switch, PG Window will match that of VCCA since both are supplied by VSYS_3V3 input voltage from pre-regulator. Customer can tighten after boot.

Rev 4 I2C_CRC_EN Error and Workaround

- What:** Setting I2C_2 FSM Trigger high to enable the I2C CRC does not work on Rev 4 of TPS6594133A
- Why:** Implementation of changes for watchdog and GPIO9 for disable watchdog pushed NVM over the memory limit
- Affected Revisions:** Only Rev 4 is impacted. This was fixed in Rev 5
- Software Workaround:** Instead of using the I2C_2 FSM trigger, please use SW workaround described on next page

